ACS APPLIED ELECTRONIC MATERIALS

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Ultrathin Ion-Sensitive Field-Effect Transistor Chips with Bending-Induced Performance Enhancement

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Cite This: *ACS Appl. Electron. Mater.* 2020, 2, 2601−2610 Read Online

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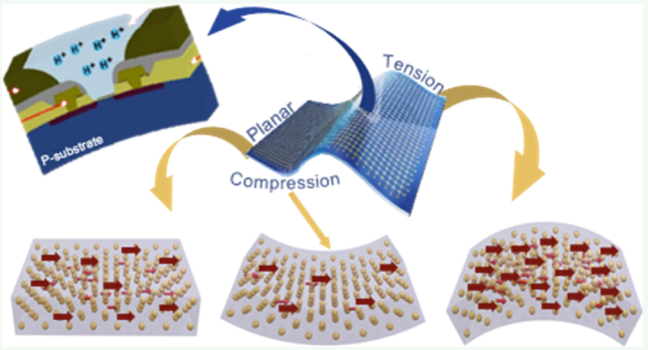
ABSTRACT: Flexible multifunctional sensors on skin or wearables are considered highly suitable for next-generation noninvasive health care devices. In this regard, the field-effect transistor (FET)-based chemical sensors such as ion-sensitive FETs (ISFETs) are attractive as, with the ultrathin complementary metal oxide semiconductor technology, they can enable a flexible or bendable sensor system. However, the bending-related stress or strain could change the output of devices on ultrathin chips (UTCs), and this has been argued as a major challenge hindering the advancement and use of this technology in applications such as wearables. This may not be always true, as with drift-free ISFETs, we show that bending could also enhance the performance of UTCs. Through fine control of bending radius in the micrometer scale, the mechanically flexible RuO_2-based ISFETs on UTCs (44.76 μm thickness) are shown to reproducibly enhance the performance even after 1000 bending cycles. The 1.3 orders of magnitude improved stability (the drift rate changed from −557 nA/min to −28 ± 0.16 nA/min) is observed over a time period of 417.3 s (~7 min) at fixed biasing and temperature conditions and under different pH conditions. Finally, a compact macromodel is developed to capture the bending-induced improvements in flexible ISFETs. The performance enhancement by controlled bending of devices could generally benefit the rapidly growing field of flexible electronics.



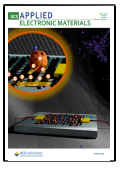
KEYWORDS: *ISFET, ultrathin chips, flexible electronics, CMOS, drift compensation*

INTRODUCTION

Flexible electronics hold great promise for several emerging applications such as smart eSkin,[1−3] wearable systems,[4,5] diagnostics tools,[6−8] noninvasive health monitoring devices,[9,10] and so forth. However, conformability is needed along with high performance and adaptability. Among a wide range of flexible chemical sensors explored for health monitoring, the field-effect transistor (FET)-based sensors such as ion-sensitive FETs (ISFETs) are attractive as they enable full system on chip using the complementary metal oxide semiconductor (CMOS) technology.[11] Further, with advances in the ultrathin chip (UTC), it is possible to realize flexible or bendable sensing systems.[12,13] In this regard, ultrathin silicon chips (UTCs) and various thin-film organic and inorganic material-based electronics have been investigated for stand-alone devices or hybrid microsystems.[14,15] However, owing to piezoresistive effects, the bending-induced variations in the output of devices on UTCs pose a major challenge in terms of their usage[16,17] in applications such as wearables where bending is essential. Few attempts made to overcome this issue include embedding the devices and circuits in the neutral plane,[18,19] the optimized channel orientation of devices during circuit layout,[20] and the use of distributed islands of rigid and stiff electronic components on flexible and stretchable substrates.[21,22] Although these attempts have yielded modest results, they also come with fabrication-related challenges. For example, practically, it is very difficult to ensure the fabrication of devices on a neutral plane. This is not the end though, as with controlled bending, the induced variations in the device response can be modulated to obtain the desired outcomes (e.g., enhance the performance) and thus develop transformative opportunities (Figure 1). Here, we demonstrate this new approach through the drift-free response of ISFETs on UTCs.

An ISFET, a semiconductor-based chemical sensor widely used in biochemical sensing applications for label-free detection of H^+ ions,[23−26] is traditionally known to exhibit instability effects because of the slow drift in the operating point of the device. The drifting phenomenon in ISFETs has

Received: June 10, 2020
Accepted: July 12, 2020
Published: July 13, 2020



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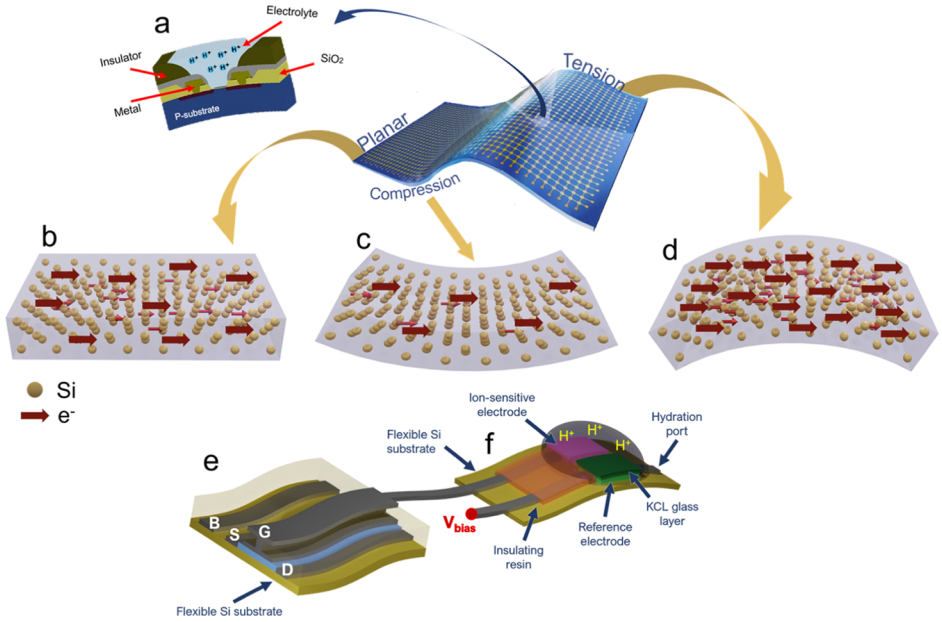

Figure 1. Illustration of electrical conductance modulation due to change in the piezoresistance of silicon. (a) Vision of this work including an array of ISFETs on flexible CMOS chips interfaced on a hybrid flexible system experiencing different bending conditions. (b) Illustration of the current density in the channel region of an n-channel MOSFET during planar conditions. (c) Illustration of the current density in the channel region of an n-channel MOSFET during compressive bending. (d) Illustration of the current density in the channel region of an n-channel MOSFET during tensile bending. (e) EG-ISFET configuration used in this work where the mechanically flexible MOSFETs are connected to the flexible silicon substrate on which the RuO_2-based ion-sensitive material and the RE were fabricated.

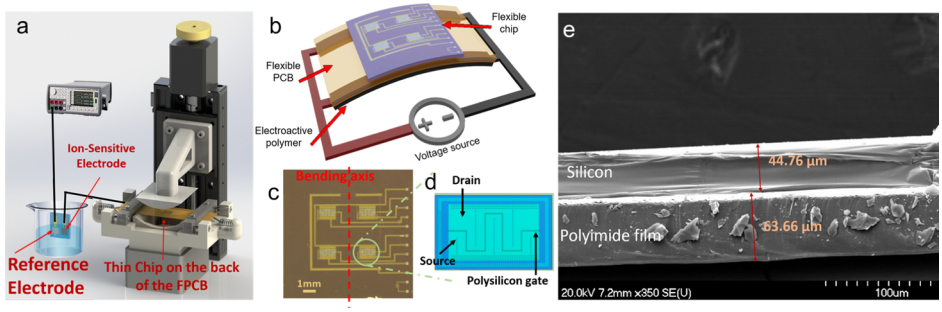

Figure 2. Experimental setup and the fabricated thin chips. (a) Schematic of the experimental setup showing the fabricated ion-sensitive gate and RE connected with the transistor on the FPCB in an extended-gate configuration. The PCB is mounted on the custom-made automated 3D-printed bending setup. (b) Schematic representation of an alternative way to bent chip using an electroactive polymer embedded on the backside of the FPCB. (c) Fabricated chip (1×1 cm^2) with four n-channel transistors and the bending axis. (d) Designed fingers of the transistor with a channel dimension of W/L = 2000 μm/12 μm. (e) Scanning electron microscopy image of the cross section of thin chip on the polyimide-based FPCB showing the thickness of the chip and FPCB.

been established through numerous studies, the fundamental effect of the composition of sensing materials, and the biasing of the electrolytic solution.[27,28] In addition, the fabrication-induced trapped charges, the attenuation of the signal due to additional passivation capacitances, and the leakage across the reference electrode (RE) could all contribute to the overall instability of ISFETs. Also, the dynamic changes in the electrolytic solution and the low mobility of OH^- through the microstructures of the ion-sensitive material make the compensation of drift, especially in alkaline solutions, a significant bottleneck. Using this fundamental understanding, a few attempts have been made to demonstrate the real-time tuning of drift effect. These include the stacking of high-k ion-sensitive materials, the use of external signal postprocessing techniques, and the on-chip circuit implementations[29−35] (see Supporting Information Section S8). However, drift is a stochastic and dynamically evolving phenomenon by its nature, which depends on several environmental, storing, pH, and sensing material-related parameters. Therefore, it is challenging to design reliable and robust sensing microsystems that are capable of prolonged drift compensation without corrupting the pH signal and can be used for a wide range of pH sensing taking also into account all, or most, of the possible (process, voltage, and temperature) parameters that can affect the performance of ISFETs.

In this regard, mechanical means such as bending-induced changes in device response can offer a reliable alternative and also complement the aforementioned techniques to control the drift in real time. Here, by exploiting the piezoresistive nature of silicon, we present the first demonstration of real-time active drift compensation by reversible electrical conductance modulation of an extended-gate ISFET (EG-ISFET) on UTCs.

The experiments were designed with a RuO_2-based ion-sensitive electrode deposited on a thin and bendable silicon

https://dx.doi.org/10.1021/acsaelm.0c00489
ACS Appl. Electron. Mater. 2020, 2, 2601−2610

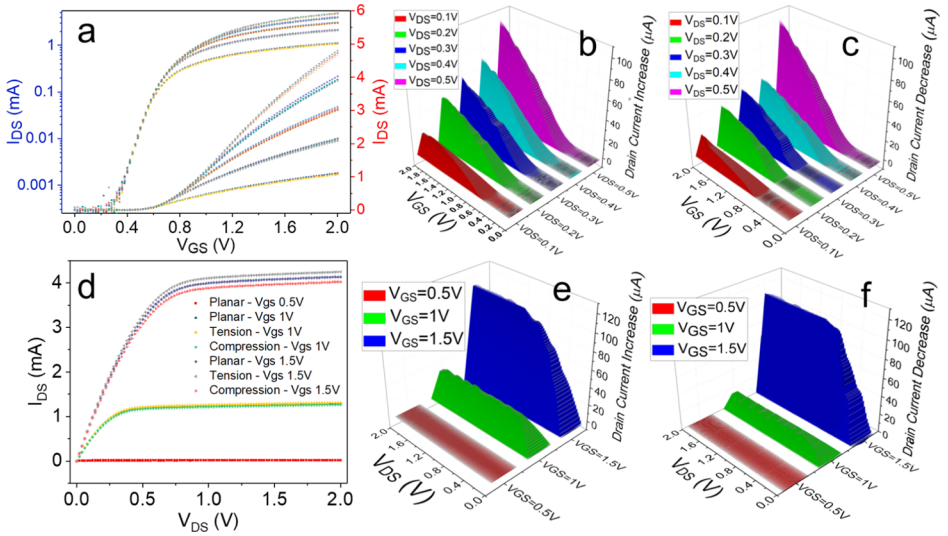

Figure 3. *I*–*V* characteristics of the fabricated bendable transistors. (a) Transfer characteristic of MOSFET (also shown in a semi-logarithmic scale) at planar, 21 × 10^{-4} nominal compressive strain, and 21 × 10^{-4} nominal tensile strain bending conditions at different drain voltages (0.1, 0.2, 0.3, 0.4, and 0.5 V). (b) Visualization of drain current increase when the fabricated MOSFETs experience 21 × 10^{-4} nominal tensile strain at the same drain voltages used in (a). (c) Visualization of drain current decrease when the MOSFETs experience 21 × 10^{-4} nominal compressive strain at the same drain voltages used in (a). (d) Output characteristics of MOSFET at planar, 21 × 10^{-4} nominal compressive strain, and 21 × 10^{-4} nominal tensile strain bending conditions at different gate-voltages (0.5, 1, and 1.5 V). (e) Visualization of drain current increase when the MOSFETs experience 21 × 10^{-4} nominal tensile strain at the same gate voltages used in (d). (f) Visualization of drain current decrease when the MOSFETs experience 21 × 10^{-4} nominal compressive strain at the same gate voltages used in (d).

substrate. In addition, a RE was deposited on the same bendable silicon substrate to obtain a compact device. The bendable ion-sensitive electrode was then connected with a thin and bendable n-channel transistor, as shown in Figure 1e,f. Both the silicon substrates (having the same thickness) were bent at various bending radii. RuO_2-based pH sensors were reported in the past and exhibit good chemical stability and restrained space charge accumulation close to Nernstian response (59 mV/pH) in a wide range of pHs.[36] However, potentiometric measurements of RuO_2-based sensors show slow response in neutral and basic solutions, which leads to an increase in drift time. Correlating the applied strain with electrical measurements reveals a detailed mechanism with which the system transforms into a controllable and reversible electrical conductance modulator targeting real-time active drift compensation irrespective of the evolution of drift's behavior over time.

RESULTS

MOSFET Characterization and Bending-Induced Strain Analysis. The fabricated and mechanically flexible devices (Figure 1) were characterized after placing them on a custom-made high-quality three-dimensional (3D) printed bending setup for compressive (downward direction) and tensile (upward direction) uniaxial bending stress, as shown in Figure 2. Uniaxial deformation happened as a force applied transversely along the middle line of the UTC caused it to bend along an in-plane axis (i.e., *x*-axis or *y*-axis), as shown in Figure 2d, resulting in an effective increase of the device's channel width (W) from 2000 to 2003.638 μm at its maximum bent state (i.e., 40 mm bending radius) while its 12 μm length (L) remained unchanged. In our case, because the stacked layers have almost similar thicknesses, the total strain in the location y of the multilayer can be formulated as[37]

$$\varepsilon = c + \frac{y - t_b}{R_c} \quad (1)$$

where c is the uniform strain component on the individual layers mainly because of the thermal expansion and R_c is the bending radius. The parameter t_b is the location of the bending axis of the trilayer structure (PI, epoxy, and silicon) where the strain is null and is given by

$$t_b = \frac{\sum_{i=1}^{n} E_i t_i (2h_{i-1} + t_i)}{2\sum_{i=1}^{n} E_i t_i} \quad (2)$$

where E_i is Young's modulus of the respective layer, t_i is the thickness of the respective layer, and h_i is the distance between the first layer and the ith stacked layer. Using eqs 1 and 2, the total strain that the thin transistors (Figure 2c) experience at 40 mm bending radius is calculated to be −21 × 10^{-4} for compressive and +21 × 10^{-4} for tensile bending stress, respectively. A detailed discussion about the calculation of strain at different bending radii is given in Supporting Information Section S2. The strain was calculated by considering that Young's modulus of polyimide, epoxy, and silicon are 8.5, 2.1, and 140 GPa,[38] respectively. After packaging of the thin fabricated chips (for details, see the Materials and Methods section), they were mounted on an automated 3D-printed bending setup (Figure 2a). Initially, we evaluated the drift of the fabricated n-channel metal oxide semiconductor FETs (MOSFETs) and the results are given in Supporting Information Section S3. Subsequently, using the bending setup, we evaluated the effects of bending on the fabricated transistors' threshold voltage and drain current. The transfer and output characteristics ($I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$) of the flexible MOSFETs and the increase/decrease in current due to bending are shown in Figure 3. Under tensile stress, the decrease in the output resistance of n-type metal oxide semiconductor (NMOS) devices and the increase in their gate

https://dx.doi.org/10.1021/acsaelm.0c00489
ACS Appl. Electron. Mater. 2020, 2, 2601−2610

capacitance leads to an increase in the drain current (I_{DS}) of the devices.[39] The opposite happens during the compressive stress. The increase or decrease of I_{DS} while applying an external strain also results from the increase or decrease of the effective device's channel area ($W \times L$) at different bending states. Finally, an additional factor of electrical conductance enhancement or suppression under bending conditions is the biasing conditions of the device. As shown in the transfer and output characteristics (Figure 3) of bendable MOSFETs obtained at a different drain−source voltage (V_{DS}) and gate−source voltage (V_{GS}), the higher degree of relative change in drain current of the bent devices was measured at higher V_{DS} and V_{GS}. Such a mesoscopic disorder results from an increased electric field between drain and source at higher V_{DS} while the device is operating in the linear region. In this region of operation, I_{DS} is proportional to $V_{DS,}$ and any bending-induced shift in the mobility (μ), threshold voltage (V_{TH}), oxide capacitance (C_{ox}), and channel area ($W \times L$) of the transistor will result in a proportionally increased shift of I_{DS} at higher biasing V_{DS} voltages. In addition, while the device operates in the linear region, a decreased output resistance (r_{out}) at higher overdrive voltages ($V_{GS} - V_{TH}$) also contributes in the relatively higher accumulation of extra charges upon bending, leading to increased bending-induced shift of I_{DS}.

Ion-Sensitive Gate Characterization. The extended-gate structure used in this paper offers greater flexibility in terms of investigation as it is possible to decouple the effects of mechanical bending from those related to chemical interactions on the potentiometric ion-sensitive electrode. This allows us to quantify separately the shift in threshold voltage due to bending stresses, changes in the pH of the solution, and drifting of the produced potential from the ion-sensitive electrode. In addition, the extended-gate configuration offers advantages such as the prevention of damage of the electronic components due to potential leakage of the liquid under test and the replaceability only of the extended ion-sensitive electrode after each chemical or biological experiment while keeping the same ultrathin silicon chip, which can operate for up to 1000 bending cycles. Further, RuO_2 has a higher Young's modulus than silicon (252 vs 140 GPa), and for that reason, we sought here to take full advantage of the mechanical flexibility of the silicon die by separating them in an extended-gate configuration. It may be noted that the CMOS-based ISFETs integrated into large numbers with front-end electronics are essentially EG-ISFETs. Therefore, this study of an extended-gate configuration and device modeling is useful for circuit designers, who could simulate the performance of their ISFET-based application-specific integrated circuits at different bending and pH conditions. For similar reasons, the extended-gate architectures have also been used in physical sensing applications such as pressure and touch sensors.[40]

The RuO_2-based ion-sensitive electrode and the Ag-/AgCl-/KCl-based RE were fabricated using screen-printing[41] on the same thin and flexible (45.72 μm thick) Si substrate which was subsequently connected in an extended-gate configuration with the bendable NMOS transistors, as shown in Figure 1e (see Supporting Information Section S1 concerning the fabrication steps). The ion-sensitive electrode and REs were also characterized before and after 1000 bending cycles, and the results are given in Supporting Information Section S1. The initial sensitivity of the RuO_2-based electrodes which was −40.7 mV/pH for a range of pH between 4 and 9 was not altered more than 0.03% after 1000 bending cycles at a maximum bending radius of 40 mm. This indicates that the performance of ISFETs cannot be affected because of the bending of the ion-sensitive material at 40 mm bending radius but only because of the change in the piezoresistance of the silicon substrate. The sensitivity measurements were obtained using the Metrohm Autolab PGSTAT128N, and the EG-ISFET characteristics were obtained using the Keysight B2912A precision source/measure unit.

Theoretical Modeling. CMOS-compatible ISFETs, and in general EG-ISFETs, consist of an ion-sensitive layer usually composed of a metal oxide and deposited on top of a MOSFET structure, which is fabricated by extending the intrinsic polysilicon gate. In general, an ISFET has the same operation as an MOSFET device except that the ion-sensitive gate is exposed to a chemical solution and influenced by a reference voltage. Here, we model the fabricated EG-ISFET as a CMOS-compatible floating gate ISFET because they have essentially the same structure. ISFETs require a RE to bias the electrolyte−insulator interface to a defined potential so that shifts in the flat-band voltage due to pH variations to be able to be measured. Every ion-sensitive material used as a gate exhibits a different sensitivity to H^+ ions, which can be expressed as a function of the double-layer capacitance and intrinsic buffer capacity of the oxide. The physicochemical macromodels of ISFETs reported in several studies[42−44] consider ISFETs as two stages coupled together: the electrochemical stage (i.e., the electrode−electrolyte interface) and the electronic stage (i.e., the transistor). However, none of the reported models have considered the effects of external mechanical bending.

For the first stage of the ISFET behavioral model (i.e., the electrochemical stage), to understand how the pH sensitivity of the metal oxide is affected and thus the electrical conductance of our ISFET, we perform the principles of proton adsorption and the formation of the electrical double-layer (EDL) theory at the surface of the ion-sensitive dielectric by using the site dissociation model introduced by Yates et al.[45] and the Gouy−Chapman−Stern theory,[46] respectively. When RuO_2 is immersed into a solution, the surface is hydrated by the dissociative adsorption of water, previously observed using X-ray photoelectron spectroscopy. Based on the reversible intercalation reaction and the investigation of point-of-zero charge,[47−49] the mechanism that explains RuO_2 sensitivity in pH is

$$RuO_x(OH)_y + ze^- + zH^+ \leftrightarrow RuO_{x-z}(OH)_{y+z}$$

which can be simplified to

$$Ru^{IV}O_2 + e^- + H^+ \leftrightarrow Ru^{III}O(OH)$$

By following the calculation steps described previously in ref 50 (see also Supporting Information Section S4 for a detailed explanation of the model), the electrolyte−oxide surface potential, which varies with the pH value of the solution, can be calculated as a function of pH and surface potential as follows:

$$V_{chem} = f(pH, V_{chem}) \quad (3)$$

For the second stage of the ISFET behavioral model (i.e., the electronic stage), we consider that in planar conditions, the ellipsoidal shape of the six degenerated valleys (Δ_6) of the conduction band structure of crystalline silicon along the

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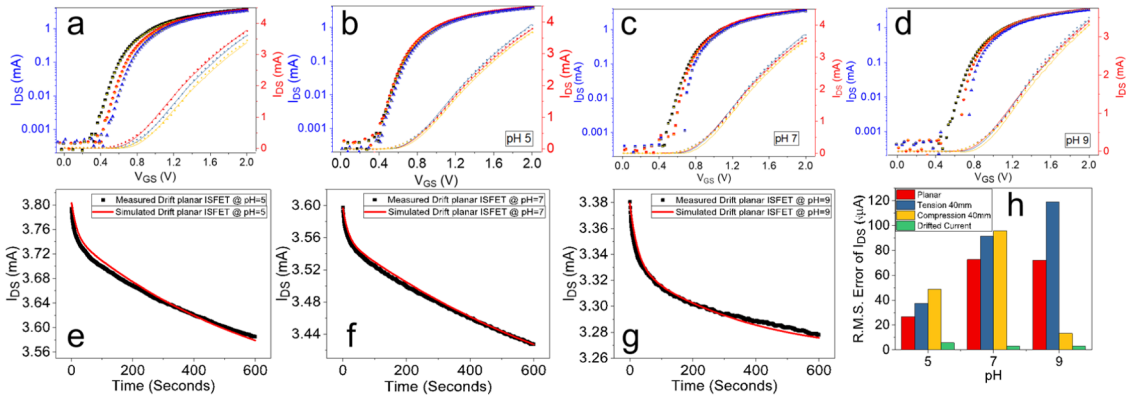

Figure 4. Experiment and simulated $I-V$ and $I-t$ characteristics of the thin and bendable EG-ISFETs. (a) Measured (compact lines) and simulated (dotted lines) ISFET transfer characteristics at pH 5, 7, and 9 at planar condition. Measured transfer characteristics are also shown in a semilogarithmic scale with dotted lines. (b) Measured (compact lines) and simulated (dotted lines) ISFET transfer characteristics at pH 5 under planar (red line), 21 × 10^{-4} nominal compressive strain (yellow line), and 21 × 10^{-4} nominal tensile strain (blue line). Measured transfer characteristics are also shown in a semilogarithmic scale with dotted lines. (c) Measured (compact lines) and simulated (dotted lines) ISFET transfer characteristics at pH 7 under planar (red line), 21 × 10^{-4} nominal compressive strain (yellow line), and 21 × 10^{-4} nominal tensile strain (blue line). Measured transfer characteristics are also shown in a semilogarithmic scale with dotted lines. (d) Measured (compact lines) and simulated (dotted lines) ISFET transfer characteristics at pH 9 under planar (red line), 21 × 10^{-4} nominal compressive strain (yellow line), and 21 × 10^{-4} nominal tensile strain (blue line). Measured transfer characteristics are also shown in a semilogarithmic scale with dotted lines. (e−g) Measured and simulated ISFET transient response at pH 5, 7, and 9 at planar condition. (h) rms error between measured and simulated results. All measurements and simulations were performed at $V_{RE} = V_{GS} = 2$ V and $V_{DS} = 0.4$ V.

[100], [001], and [010] crystal orientation has two different effective masses (i.e., longitudinal: $m_l = 0.97m_0$, and transversal: $m_t = 0.19m_0$, where m_0 is the free electron rest mass). As the externally applied stresses increase, repopulations of electrons into the split conduction sub-bands Δ_4 and Δ_2 will affect the effective mass (m^*) and the momentum relaxation time (τ). As the carrier mobility is expressed by $\mu = \frac{|\vec{v}|}{|\vec{E}|} = \frac{q \times \tau}{m_0 \times m^*}$, any change in m^* and τ will change the mobility and thus the resistivity of silicon. Along with mobility, the threshold voltage (V_{TH}) and the drain current (I_{DS}) of the ISFET also change. In previous works, we formulated analytical equations relating the stress with the drain current and threshold voltage.[5,26] By using the modified drain current and threshold voltage equations of the MOSFET shown below, the second stage of the ISFET behavioral model was implemented in Verilog-A and simulated in the Cadence Virtuoso environment.

$$I_{DS(stress)} = I_{DS_0}(1 \pm \Pi_{I_{DS}} \times \sigma_{I_{DS}}) \quad (4)$$

$$V_{TH(stress)} = V_{TH_0}(1 \pm \Pi_{V_{TH}} \times \sigma_{V_{TH}}) \quad (5)$$

where I_{DS_0}, V_{TH_0}, $I_{DS(stress)}$, $V_{TH(stress)}$, $\Pi_{I_{DS}}$, $\Pi_{V_{TH}}$, and σ are the drain current and threshold voltages in planar conditions, the drain current and threshold voltages under bending conditions, the piezoresistive coefficients proportional to the drain current and threshold voltage, and the magnitude of stress, respectively. A comparison between the modeled and experimental transfer characteristics of ISFET at different pH conditions and under different bending strains is presented in Figure 4. As noted above, based on previous reports, there is a strong likelihood of the existence of drift effect in the RuO_2 pH sensitivity especially in alkaline solutions, which can last up to several days, resulting in limitation of accuracy and precision of ISFET-based microsystems. In this context, when a metal−oxide (M−O_X) is exposed in an aqueous solution, OH^- sites are slowly formed on the surface of M−O_X[51] and propagate down to a depth of tens of angstroms, giving rise to slow temporal growth of the hydrated surface layer.[52] This results in a slow monotonic temporal change of the dielectric constant of the hydrated surface layer resulting in an overall change of the electrical properties of RuO_2 including capacitance, defined as the series combination between the capacitance of the hydrated surface layer and the capacitance of rest of the bulk of RuO_2, which in turn results in a slow monotonic temporal change in the drain current of ISFET at a given $V_{RE} - V_{TH}$ voltage. Research to model this nonideal effect of drift on ISFETs has been carried out toward the development of physicochemical models[53,54] and the development of SPICE models that can be used in a CAD system.[55] To model the effect of drift and to perform device-level simulations, we have also included the effect of drift in the second stage of our behavioral model as the rate with which drain current is shifting overtime at fixed biasing (constant drain−source voltage and RE potential) and temperature conditions. The drift is modeled as a nonideal effect caused by both the surface oxidation of RuO_2 as the fast response and by the response of the buried sites as the slow response.[56] The drift rate of an ISFET's drain current (I_{DS_drift}) can be written as

$$\text{Drift\_rate} = \frac{d[I_{DS\_drift}]}{dt} \quad (7)$$

where I_{DS_drift} is given by

$$I_{DS\_drift} = s_f \times e^{(-t_f/\tau f)} + s_s \times e^{(-t_s/\tau s)} + D_c \quad (8)$$

where s_f is the maximum shift of I_{DS_drift} due to the fast response, s_s is the maximum shift of I_{DS_drift} due to the slow response, D_c is the drift coefficient, and t_f and t_s are the time intervals corresponding to the time constant of fast response (τf) and the time constant of slow response (τs), respectively. Therefore, the final equation of bendable ISFET's drain current becomes

$$I_{D(stress)} = \text{drift\_rate} \times [I_{D_0}(1 \pm \Pi_{I_D} \times \sigma_{I_D})] \quad (9)$$

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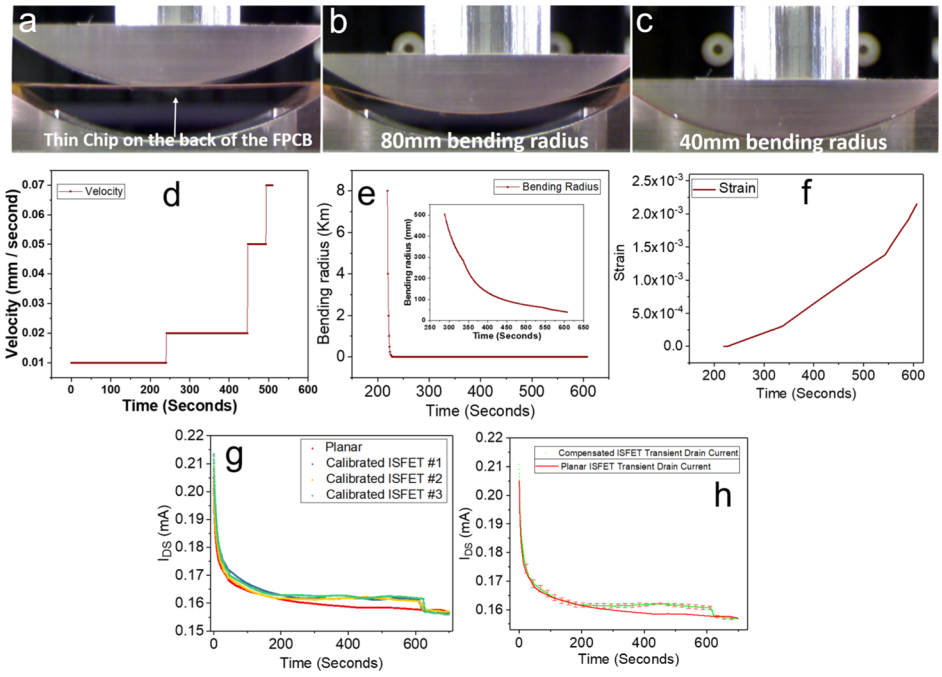

Figure 5. Photographs of the flexible chip under different bending states and plots with three different parameters to achieve drift-free response from EG-ISFETs for 7 min. (a) Motorized press at the moment of contact with the FPCB. (b) Motorized press when it has reached the mid-point of the overall traveled distance and the chip is bent under 80 mm bending radius. (c) Motorized press when it has reached a maximum traveled distance and the chip is bent at 40 mm bending radius. (d) Velocity vs time diagram of the preprogrammed movement of the motorized press. (e) Calculated bending radius vs time diagram to achieve drift-free ISFET response. (f) Calculated strain vs time diagram to achieve drift-free ISFET response. (g) Transient response of ISFET under planar condition compared with the drift-free response achieved by applying sequentially increased strain via a closed-loop control, which captures the sensor's output current and takes an appropriate decision to control the motion of the motorized press. (h) Comparison of planar and drift compensated ISFET response showing the error bars. All measurements were performed at $V_{RE} = V_{GS} = 1$ V and $V_{DS} = 0.4$ V.

The comparison between modeled and experimental drift behavior at different pH conditions is presented in Figure 4e–g and the modeled versus measured transfer characteristics are characterized by a root-mean-square (rms) error shown in Figure 4h. A detailed discussion about the model is given in Supporting Information Section S4.

Compensation of Drift by Bending the EG-ISFETs. A specialized testing system was developed to achieve precise control over the bending of the fabricated EG-ISFETs, as shown in Figure 2a. The motorized press at the moment of contact with the flexible printed circuit board (PCB) is shown in Figure 5a. Using this system, a smooth transition of the curvature of EG-ISFETs was achieved because of its capability of incremental motions in the micrometer (μm) range. Figure 5b,c shows the ISFET chip bent under 80 and 40 mm bending radii, respectively. The corresponding velocity variation with time of the motorized press is presented in Figure 5d.

A detailed mechanism thus emerges, as indicated in Figure 5d–f: as the external dynamic strain sequentially applied on a silicon substrate is increasing, an effective reduction in carrier mass occurs, which subsequently changes the charged surface carrier mobility and the resistivity of silicon (Si). This change occurs because of the modification of the electronic band structure. Microscopically, the modification stems from a reduction in the number of symmetry operations allowed, which in turn depends on the way the crystal is stressed. This breaking of the symmetry of the fcc lattice of Si can result in a shift of the energy levels of the different conduction and valence bands, their distortion, removal of degeneracy, or any combination. More specifically, during biaxial strain in the (001) plane, the 6-fold degenerate Δ6-valleys in Si are split into a 2-fold degenerate Δ2-valley pair (located along the [001] direction) and a 4-fold degenerate Δ4-valleys pair. In terms of symmetry considerations, this stress condition is equivalent to applying uniaxial stress along the [001] direction. Therefore, in a n-channel ISFET under tensile strain, the resistance of the n-type channel decreases, the gate capacitance increases, the dimensions (W/L) change, and therefore, the current of the device increases. The opposite happens in the case of compressive strain.

With the overall relative change of current, the system transforms into a controllable electrical conductance modulator targeting real-time active drift compensation. In this context, our results represent an important advance with the 1.3 orders of magnitude improved stability (the drift rate changed from −557 nA/min for planar ISFET to −28 ± 0.16 nA/min for ISFET under sequentially applied external dynamic tensile strain) over a time period of 417.3 s (~7 min) at fixed biasing and temperature conditions. The mean absolute current over this period was $161.48 \pm 5.64 \times 10^{-4}$ μA. As we have observed from the experiments, the performance of EG-ISFETs changes only because of the bending of the electronic part (i.e., transistor) and does not get affected by the bending of the ion-sensitive electrode and REs.

The plots for bending radii versus time and the calculated strain versus time that have been used to achieve a drift-free ISFET response are shown in Figure 5e,f, respectively. By using these data, we extracted eqs 10 and 11 for the bending radius and strain as a function of time to achieve a drift-free ISFET response. It should be noted that there is a nonlinear

https://dx.doi.org/10.1021/acsaelm.0c00489
ACS Appl. Electron. Mater. 2020, 2, 2601−2610

relationship between the applied strain and the cancellation of drift.

$$\text{Bending radius}(t) = \text{BR}_1 \times e^{[-(t-t_0)/t_1]} + \text{BR}_2 \times e^{[-(t-t_0)/t_2]} + \text{BR}_3 \times e^{[-(t-t_0)/t_3]} + C_{\text{BR}} \quad (10)$$

$$\text{Strain}(t) = S_1 \times t + S_2 \times t^2 + S_3 \times t^3 + S_4 \times t^4 + S_5 \times t^5 + C_s \quad (11)$$

The transient response of ISFET under planar conditions is also compared with the drift-free response (Figure 5g) achieved by applying a sequentially increased strain using the proposed closed loop system. The comparison of planar and drift-free ISFET response showing the error bars is presented in Figure 5h. The main advantage of using transistors on flexible silicon (Si) substrates is that the effect of bending on their performance is reproducible even after 1000 bending cycles. The experiments to check the repeatability of the effect of bending on the devices are discussed in Supporting Information Section S5. In addition, from the experiments analyzed in Supporting Information Section S6, we note that the drift rate does not change when the device is under strained conditions.

DISCUSSION

The bending-induced controlled modulation of device response gives a new perspective to using the stress engineering of UTC-based microsystems. Also, the device characterization during automated sequential bending of silicon can provide useful information about the transistor that is undergoing bending and can be considered as useful performance evaluation and failure analysis tool. We have demonstrated that not only does the relative shift in electrical conductivity of an ISFET depends on the applied nominal strain but it also depends on the biasing conditions of the transistor and it does not depend on the mechanical deformation of the electrolyte−insulator interface. In addition, it was observed that the relative rate of change of drain current during sequentially applied mechanical stress has a nonlinear behavior as the strain gradually increases. Our experiments and calculations suggest that even after 1000 bending cycles at the maximum tested nominal stain of $\pm 21 \times 10^{-4}$, the mechanically flexible Si-UTC-based system can be reliably used as a reversible electrical conductance modulator maintaining its durability after multiple mechanical deformations.

Furthermore, the sensitivity of RuO_2 is unaffected (0.03%) after 1000 bending cycles tested under the same maximum nominal strain ($\pm 21 \times 10^{-4}$). Therefore, in cases where drift follows a downward slump, a tensile strain can be externally applied to compensate for drift. The opposite applies when drift follows an upward slope (see Supporting Information Section S7). In addition, we note that the drift rate does not change under strained conditions, which is a rather intuitive result because drift is associated only with the diffusion of hydrating species within the bulk of the ion-sensitive material. We also note that when the flexible ISFETs are already strained at the maximum convex bending radius of 40 mm at the start of the measurement, the initial fast drop of drain current lasts less time compared to the time elapsed when ISFETs are at the planar condition at the beginning of the measurement.

The drift by nature is a stochastic and dynamically evolving phenomenon dependent on the ambient temperature, storing conditions, the stabilization of EDL, the ion-sensitive material used each time, and the pH of the solution under test, to mention a few. Thus, it is challenging to engineer a system that can compensate for all or most of the possible variabilities in the system. With this study, we demonstrate that nonlinear bending of the chip leads to the cancelation of drift and we propose a closed loop compensation system which captures the sensor's output current and takes an appropriate decision to control the speed of the motion of the motorized press, allowing real-time drift compensation and better control of the compensation process, irrespective of the sensor's variabilities and drift's evolving behavior over time. Also, the modeling of mechanically bendable ISFETs on UTCs is important for designing mechanically flexible circuits as the electrical conductivity variations induced by bending could be included in the CAD models to simulate and evaluate the performance of the circuits. From a practical standpoint, we have designed and built a compact low-cost 3D-printed automated bending setup of overall size 10×12 cm^2, which can accommodate the full range of displacement of the motorized press. The motorized press was operated by a high-resolution linear actuator, capable of incremental motions in the micrometer (μm) range allowing fine control of bending radius. However, we note that bending of the chip can also be achieved with soft actuators such as electroactive polymers, shape memory alloys, or pneumatic actuators embedded on the backside of the flexible PCB (FPCB),[57] as shown in Figure 2b, to further reduce the size and increase the versatility of the system. To further reduce the size of the system, we have fabricated the RE on-chip,[58,59] avoiding the use of bulky external glass-based REs. The proposed system can be integrated into robots used in remote harsh environments (e.g., space applications) or for laboratory analysis such as continuous pH measurement of blood. The demonstrated method can offer a reliable alternative or complementation of the aforementioned drift compensation techniques discussed earlier.

CONCLUSIONS

In summary, we have demonstrated the first CMOS-compatible RuO_2-based EG-ISFET on ultrathin silicon thinned using lapping technique and proving the capability of the proposed system to controllably compensate for the long-standing problem of drift in ISFETs. We show large reversible conductance modulation with a maximum change of 2.34% in EG-ISFET's drain current and with 1.3 orders of magnitude improved stability (the drift rate changed from −557 nA/min for planar ISFET to -28 ± 0.16 nA/min for ISFET under sequentially applied external dynamic tensile strain) over a time period of 417.3 s (~7 min) when the device experiences sequentially applied external bending strain up to 21×10^{-4}. Using a low-cost custom-made automated 3D printed three-point bending setup, we reveal the ability to actively flex the silicon chip while it is operating to achieve a drift-free response under different pH conditions. Sequential bending of the chip during operation provides a direct link between the applied strain and the electrical conductance modulation due to change in the piezoresistance of silicon. Finally, a mathematical model was developed in a CAD tool, which can predict the effects of pH, bending, and drift on the performance of the

https://dx.doi.org/10.1021/acsaelm.0c00489
ACS Appl. Electron. Mater. 2020, 2, 2601−2610

fabricated EG-ISFET and can be used in circuit-level simulations for applications that require bendable integrated circuits.

MATERIALS AND METHODS

MOSFET Fabrication. The structure of EG-ISFETs used in this work is shown in the schematic of Figure 1. The electronic part of ISFET (i.e., the transistor) was fabricated on a double-side-polished n-type 6″ wafer. The p-well was implanted using boron (B11) as a dopant with a dose of 650 × 10^{12} atoms/cm^2 and an energy of 100 keV through a screen oxide of 20 nm thickness. Annealing was performed in a nitrogen ambient atmosphere for 11 h at 1150 °C. The buffer oxide was grown at 975 °C in a dry oxygen ambient atmosphere for 45 min to achieve a thickness of 50 nm. Subsequently, nitride and oxide were deposited using low-pressure chemical vapor deposition, followed by etching of the nitride to define the active area at the front side. The field oxide was then grown in a wet oxygen ambient atmosphere at 975 °C for 9 h, and the channel threshold adjustment implant was performed through the screen oxide. Polysilicon with a thickness of 450 nm was then deposited using pressure-enhanced chemical vapor deposition at 620 °C and patterned to define the gate area following the definition of the well contact, which was formed by implanting BF_2 at a dose of 5 × 10^{15} atoms/cm^2 at 80 keV energy. Successively, the source and drain regions were formed by implanting phosphorus with a dose of 5 × 10^{15} atoms/cm^2 and an energy of 80 keV, followed by implantation of arsenic with a dose of 2 × 10^{15} atoms/cm^2 and energy 120 keV. The contacts were formed by initially using plasma-etching, followed by an oxide etch-dip before metal deposition. Next, Ti/Al:Si (60/600 nm) was sputtered at room temperature. After sintering of contacts, a layer of protective overglass (SiO_x) was deposited over the wafer. Finally, the contact pads were opened. The transistors were designed and fabricated with a W/L ratio of 2000 μm/12 μm, as shown in Figure 2e.

Thinning and Packaging of Flexible ICs. Bendability can be achieved by thinning down the chips to approximately 50 μm. However, bendability is also related to the surface area of the silicon substrate; the higher the surface area, the more the thickness of the chip can be to achieve the same bending curvature. The three main processes of thinning are based on physical, chemical, or chemo-mechanical thinning techniques.[12] For this work, the silicon (Si) chips were thinned down to 45 μm using a chemomechanical thinning process termed as "lapping" technique using a bench-top PM5 Logitech precision lapping and polishing machine to ensure faster material removal (etch rate of ∼9 μm/min) with high yield if properly maintained, using abrasive as well as colloidal polishing slurry.[60] The etch rate during lapping depends on the force that is applied on the sample during lapping, the size of the alumina particles in the slurry, and the rotations per minute of the plate. In comparison with grinding, there is no need for an extra stress-relieving step such as slow ion etching or chemical−mechanical polishing because during lapping, the sample was polished as the last step of the thinning process without removing it from the sample-holding jig. In addition, there is no need for a protection tape commonly used in grinding, which can increase the probability of breakage of thinned wafers and chips during their delamination of the tape. Instead, it was used as a thin film (1 μm) of bonding wax with a melting point of 75 °C. Finally, the thin chips were packaged on 63.66 μm thick polymeric FPCBs using low-stress EpoTEK 301-2 epoxy glue with Young's modulus and Poisson's ratio of 2.1 and 0.358 GPa, respectively. The epoxy consists of two parts which were mixed in a ratio by weight of 100:35. A small drop of epoxy was placed and spread on the backside of the thinned chip using a tool with a fine tip, and the thin chip was then transferred and carefully placed on the FPCB using a pick-and-place tool to avoid air gaps between the chip and the FPCB. The thin die was then gently pushed with the same tool to ensure that the epoxy was spread uniformly throughout the backside of the chip. In that way, a small amount of epoxy could flow from the sides of the chip avoiding having an excess of epoxy, resulting in a chip that will "swim" away. It should be noted that the viscosity of the epoxy is very low (225−425 cPs), allowing most of its excess to flow out from the sides. After carefully removing the residues of the epoxy preventing them to spread on the front side of the die, the system was heated up to 80 °C for 3 h to allow the epoxy to cure. Finally, after letting the system to cool at room temperature, the chip was wire-bonded using the ball to wedge technique.

Custom-Made Automated 3D Printed Bending Setup. A specialized testing system was developed to achieve precise control over the bending of the EG-ISFET. The system comprised two main components, a holding bracket for the FPCB and a motorized press. At the interface, a pair of interlocking curved parts with a 40 mm radius was fitted. These components were manufactured in-house using a high-precision 3D printer and ensured that the ISFET would reach the maximum required curvature. The top press was operated by a high-resolution linear actuator, capable of incremental motions in the micrometer (μm) range. The bottom holding bracket employed a set of springs which maintained the tension in the PCB during the test, thus ensuring a conformal contact with the upper press. Using the designed system, a smooth transition in the curvature of the ISFET was achieved.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.0c00489.

Detailed fabrication and characterization method of the rigid and flexible ion-sensitive electrode and REs; mathematical explanation of the calculation of bending radius and strain based on the obtained experimental data; characterization of the fabricated transistors' drift; detailed mathematical formulation of the ISFET macro-model implemented in Verilog-A; experiments proving the repeatability of the effect of bending on the performance of ISFETs on ultrathin silicon chips; experiments proving that the relative shift in electrical conductivity of flexible ISFETs on UTCs depends on the applied nominal strain and on the biasing conditions but does not depend on the mechanical deformation of the electrolyte−insulator interface; experiments showing improvement in the performance of ISFETs on ultrathin silicon chips as the pH of the solution changes in real time; and reported drift compensation techniques (PDF)

Behavior of drift in bendable EG-ISFETs (MP4)

Compensation of drift by bending the EG-ISFETs (MP4)

Repeatability of bending effect on EG-ISFETs (MP4)

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https://dx.doi.org/10.1021/acsaelm.0c00489
ACS Appl. Electron. Mater. 2020, 2, 2601−2610

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Author Contributions

R.D. and A.V. conceived the idea and A.V. carried out the fabrication, simulation, and characterization of the ISFET chip. A.C. developed the custom-automated 3D-printed bending setup. A.V. and A.C. performed the experiments for the drift compensation of EG-ISFETs. L.M. synthesized the RuO_2 paste and fabricated the sensor. All authors contributed to manuscript writing, with overall supervision of the work provided by R.D.

Notes

The authors declare no competing financial interest.

The data that support the findings of this study are available from the corresponding author upon reasonable request.

■ ACKNOWLEDGMENTS

This work was supported in part by EPSRC through Engineering Fellowship for Growth (EP/M002527/1 and EP/R029644/1) and Centre for Doctoral Training in Intelligent Sensing and Measurement (EP/L016753/1). The authors are thankful for the support received for this work from the members of BEST group at the University of Glasgow, the James Watt Nanofabrication Centre (JWNC), and the Glasgow Electronic Systems Design Centre (ESDC).

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https://dx.doi.org/10.1021/acsaelm.0c00489
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